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SIMULATION AND DESIGN OF AREA-EFFICIENT BUILT-IN SELF-TEST TECHNIQUE WITH MAXIMIZING TEST COVERAGE

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Abstract:
With the semiconductor industry pushing the boundaries of integrated circuit (IC) design and manufacturing, there is a greater demand than ever for reliable and efficient testing techniques. This abstract uses a novel "Area-Efficient Built-In Self-Test" (AEBIST) approach to explore the intricate link between test coverage and chip area consumption. This work's primary objective is to explore the most effective ways to maximize silicon real estate utilization while resolving the challenges associated with creating AEBIST approaches that provide complete test coverage. Traditional external testing methods sometimes cannot keep up with the increasing complexity and heterogeneity of today's integrated circuits (ICs). In response, AEBIST—which embeds independent testing circuits right into the chip—appears to be a workable substitute. The core concepts of AEBIST design are examined in this article, emphasizing the technology's inherent ability to maximize test coverage through strategic placement of test circuits that minimizes impact on chip area. Test pattern generators, signature analyzers, and efficient fault detection algorithms are used to ensure that AEBIST helps identify faults without consuming too much chip space.
The importance of adapting to AEBIST methods is also emphasized in the abstract. It discusses how these techniques can be modified to suit a range of applications, ensuring that the particular testing needs of different integrated circuits are met while maintaining area efficiency. AEBIST methodologies provide an adaptable structure for achieving superior test coverage by accommodating varying design considerations and testing goals.

I. INTRODUCTION

In recent years, with the advance of semiconductor manufacturing technology, the requirements of digital very-large-scale-integrated (VLSI) circuits which are composed of tens to hundreds of millions of gates, have led to many challenges during manufacturing test. Moreover, the unprecedented levels of design complexity and the gigahertz range of operating frequencies make the testing of nanometre system-on-chip (SOC) designs a most demanding challenge. This is because the large and complex chips require a huge amount of test data and dissipate a substantial amount of power during test, which greatly increases the system cost. The main objectives of this dissertation are: (i) To introduce novel techniques that improve the power consumption during test. (ii) To introduce novel techniques to achieve high fault coverage in the circuit under test (CUT). (iii) To combine these new techniques with already existing techniques in order to obtain further reduction in power consumption.

1.1 AUTOMATIC TEST EQUIPMENT

Automatic test equipment (ATE) is instrumentation that is used in external testing to apply test patterns to the the CUT, and to mark the CUT as good or bad according to the analysed responses

Fig. 1.1 shows a basic diagram for external testing using ATE with its three basic components:

(i) The CUT: this is the integrated circuit (IC) part which is tested for manufacturing defects.

(ii) The ATE control unit: this unit includes the control processor, the timing module, and the power module.

(iii) The ATE memory: this memory contains test patterns that will be supplied to the CUT and the expected fault free responses which are compared with the actual responses obtained from the CUT to determine whether the CUT is faulty or not

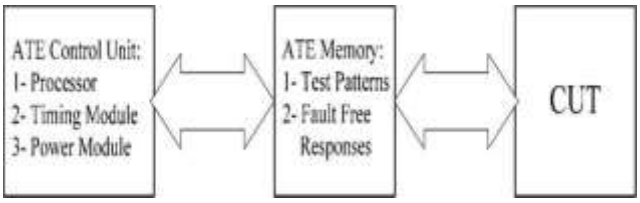

Figure 1: External testing using ATE.

External testing using ATE has a serious disadvantage since the ATE (control unit and memory) is extremely expensive and its cost is expected to grow in the future as the number of chip pins increases.

1.2 Built-In Self-Test (BIST)

As the complexity of modern chips increases, external testing with ATE becomes extremely expensive. Instead, built-in self-test (BIST) [3-6] is becoming more common in the testing of digital VLSI circuits since it overcomes the problems of external testing using ATE. BIST test patterns are not generated externally as in case of ATE; instead they are generated internally using some parts of the circuit, also the responses are analysed using other parts of the circuit. When the circuit is in test mode, test patterns generators (TPGs) generate patterns that are applied to the CUT, while the signature analyser (SA) evaluates the CUT responses.

One of the most common TPGs for exhaustive, pseudo-exhaustive, and pseudorandom TPG is the linear feedback shift register (LFSR). LFSRs are used as TPGs for BIST circuits because, with little overhead in hardware area, a normal register can be configured to work as a test generator, and with an appropriate choice of the location of the XOR gates, the LFSR can generate all possible output test vectors (with the exception of the 0s-vector, since this will lock the LFSR). The pseudorandom properties of LFSRs lead to high fault coverage when a set of test vectors is applied to the CUT compared with the fault coverage obtained using normal counters as TPGs. Also LFSRs can be configured to act as signature analysers for the responses obtained from the CUT.

Despite their simple appearance, LFSRs are based on complex mathematical theory that helps explain their behaviour as TPGs. The characteristic polynomial of an LFSR determines which flip-flop locations of the LFSR feed the inputs of the XOR gates in the feedback path. If the characteristic polynomial of an LFSR is primitive, then the LFSR will generate the maximum length non-repeating sequence ,which is called an m-sequence. LFSRs can be divided into two main categories : External-XOR LFSR and internal -XOR LFSR.These are distinguished by the way in which XORi gates are inserted into the system.

Similarly,

1.3 Standard MISR

Standard MISR is designed from a Fibonacci LFSR or external XOR LFSR where XOR gates representing the tap positions of the feedback polynomials are concatenated to produce a new output bit. This single bit output is given as feedback input to the last flip-flop in the structure. In addition extra XOR gates are inserted on to each stage of LFSR to compact all outputs on to one LFSR. The bits to be shifted to next register depends on the output of the linear gates.

BIST is one among the different techniques used for testing combinational circuits. It is a device or method that enables a machine or circuit to test itself by integrating test circuitry with the regular system circuitry to confirm the system's proper operation.

According to Fig.1.2, the Test Pattern Generator (TPG), Circuit Under Test (CUT), and Out-put Response Analyzer (ORA) are all components of BIST's overall design.

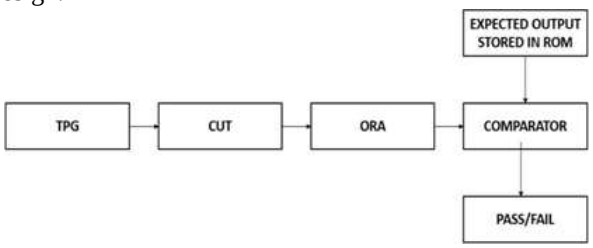

Figure 2: General Architecture of Built-In-Self -Test (BIST).

1.4 Fault Modelling

A fault model can be defined as a description of the behaviour of, and assumptions about, how components (nodes, gates. . . etc.) in a faulty circuit behave. In this way, a high percentage of faults that may occur in a circuit can be modelled. One of the most popular and common fault models at the logic level of abstraction is the stuck-at-fault model (single and multiple stuck at faults). It makes the assumption that a node under consideration is permanently connected with ground, called stuck-at-0 (sa-0), or permanently connected with Vdd, called stuck-at-1 (s-a-1). This fault model is considered to be the most common model in logic circuits. This fault model is the target fault model used throughout this thesis due to its popularity.

1.5 Power Dissipation in Digital VLSI Circuits

With the development of portable devices and wireless communication systems, design for low power has

become an important issue. Minimising power dissipation in VLSI circuits increases battery lifetime and the reliability of the circuit. In general, the power dissipation of comple-mentary metal oxide semiconductors (CMOS) circuits can be divided into two main categories: static power and dynamic power.

Static power is the power dissipated by a gate when it is inactive, i.e. when it is not switching. A significant fraction of static power is caused by the reduced threshold voltage used in modern CMOS technology that prevents the gate from completely turning off, thus causing source to drain leakage. All the components of static power dissipation have a minor contribution to the total power dissipation, and can be minimised for well-designed circuits.

1.6 Motivation for Low Power consumption

In recent years, with the fast growth of personal mobile communication and portable computing systems, design for low power has become one of the greatest challenges in high performance VLSI design. As a consequence, many techniques have been introduced to minimize the power consumption of new VLSI systems. However most of these methods focus on the power consumption during normal mode operation (functional operation) whilst test mode operation has not normally been a predominant concern. However, it has been found that the power consumed during test mode operation isi often much higher than normal mode operation because of the high switching activity in the nodes of the CUT during test.

The main motivation for considering low power testing is that a circuit consumes much more power during test than during normal mode-operation. In [19] it has been shown that the power consumed in test mode can be more than twice the power consumed in normal mode. The main reasons for this increase in test power [20, 21] are as follows: (i) In normal operation mode, if the system contains several blocks, then it is likely that only one or few of the blocks will be active at the same time, hence reducing the power consumption. By contrast, in test model parallel testing is often used to reduce test application time. This parallelism inevitably increases power dissipation during testing. (ii) The design for testability circuitry inserted in the circuit will probably be idle during normal mode but may be used intensively during test mode, hence increasing the power consumption. (iii) The correlation between the successive functional input vectors during normal operation is considered to be high compared with the correlation of test vectors in the test mode. For example, in the circuits that process digital and video signals, the inputs to most modules change relatively slowly, hence, successive inputs arei highly correlated. However, for the test vectors generated by a TPG such as LFSR, there is no definite correlation; this will increase the switching activity in the circuit.

As the excessive switching activity causes many problems ,low power testing has become a very important issue to be considered in order to avoid reliability problems and manufacturing yield loss due to high power dissipation during test in VLSI circuits.

II. LITERATURE SURVEY

A. Menbari and H. Jahanirad, "A Concurrent BIST Architecture for Combinational Logic Circuits," 2020 10thi International Conference on Computer and Knowledge Engineering (ICCKE),i 2020, pp. 262-267, do: 10.1109/ICCKE50421.2020.9303669.

The BIST techniques are divided into two categories in this paper: offline and online. A new concurrent BIST technique based on duplication design is presented in this paper. Instead of a deterministic test pattern generation (TPG) algorithm, the proposed method employs a pre- computed test set that is selected by a novel methodology. Instead of a high complex and conventional pattern detector, the proposed method uses two Linear Feedback Shift Registers (LFSR) to detect the required test patterns.

Disadvantages:

The proposed design does not address single stuck-at faults.

Parangat Mittal, Daksh Shah, "Linear Feedback Shift Register-Based Test Pattern Generators: A Comparative Study", ISSN: 2278 – 909X International Journal of Advanced Research in Electronics and Communication Engineering (IJARECE) Volume 9, Issue 8,i August 2020 60 All Rights Reserved © 2012 IJARECE

This paper attempts to compare a few recent proposals in which the Linear Feedback Shift Register (LFSR) has been suitably modified to obtain an efficient test pattern generator architecture. Pseudo Random Number Generators are widely used as Test Pattern Generators in VLSIi Design for testing digital circuits in a BIST system. The generated test pattern sequence is also useful in cryptography. It is thus critical to design an efficient test pattern generator that uses the least amount of hardware, dissipates the least amount of power, and

generates the most random sequence. This paper attempts to conduct a comparative study on previous proposals in which the LFSR has been modified or updated to produce a better Test Pattern Generator. The hardware utilisation, i.e. the number of Flip Flops (FFs) and Look-Up Tables (LUTs), and the measure of randomness of the test patterns are the parameters considered when comparing the architectures.

Disadvantages:

This paper presented a comparative analysis of three modern LFSR-based Test Pattern Gen- erators. While the design with the least hardware throughput, generates a test sequence which is less random than one with a higher hardware utilisation. A low power design,as the name suggests, dissipates lowest power but is unable to generate a truly random sequence.

Vanya Gupta ,Garimai Singh ,Abhijiti Asati , (2019)" BIST Architecture for Com- binational Circuit " ,i International Journal of Electrical, Electronics and Data Communi- cation (IJEEDC) ,pp. 1-8, Volume-7,Issue-5

In this study, testability analysis is presented using an integrated self-test (BIST). This strategy aims to fix stuck-at-fault by applying test vectors to the circuit being tested (CUT) using a test pattern generator (TPG) and recording the result using an output response compactor (ORC), with the BIST controller directing the operation of various BIST blocks. Hold logic and a component for creating signatures make up the BIST circuit. Verilog is used to simulate the BIST for the combinational logic circuit and the RTL compiler is used to implement it. Using the Serial Input Signature Register, a BIST for combinational CUT is also performed (SISR). RTL compiler is used to synthesis the designs and produce results for area, power and timing.

Disadvantages:

The synthesis results for these implementations are compared in terms of area, power, and delay. The comparison shows that SISRi require a large cell area and a high average power consumption.

III. EXISTING METHOD

3.1 SYSTEM DESCRIPTION

The majority of systems today are built with integrated test strategies like BIST, which makes use of extra hardware on the chip. The BIST replaces the conventional automatic test equipment and has a number of advantages over the earlier testing tools. A typical BIST architecture includes a test pattern generator (TPG), which is typically implemented as a linear feedback shift register (LFSR), an output response analyzer (ORA), which is typically implemented as a multiple input signature register (MISR), and a BIST control unit (BCU) all on a single chip.

3.1.1 Test Pattern Generator (TPG)

A part of BIST called a Test Pattern Generator creates test patterns for the circuit being tested (CUT). These test patterns are fed into the CUT, and each test pattern's matching outputs are received.

(i) Conventional LFSR

The traditional LFSR is the TPG that is most frequently used in BIST [1]. A N-bit conventional LFSR can produce 2N−1 patterns. Due to the random nature of the patterns it generates, this sort of TPG is also known as pseudo-random TPG. The all-zero pattern is not possible with this TPG.A typical n-bit LFSR can be seen in Fig.3.1 (external). The power is also high since there are many transitions in the patterns produced by traditional LFSR. Therefore, it would be ideal to find a way to alter the LFSR structure so that the outputs can be rearranged to decrease switching activity without affecting fault coverage. As a result, the bit-swapping technique is presented and added to the traditional LFSR

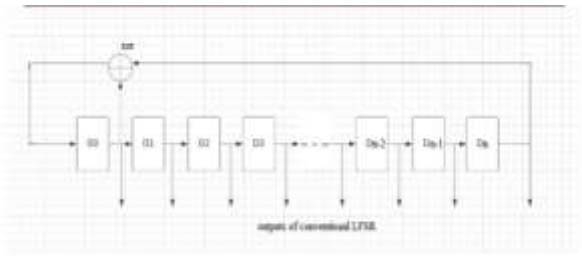

Figure 3: n-bit conventional LFSR

(ii) Bit-swapped LFSR

Bit swapping is a method for lowering switching activity, or the number of transitions. As the number of transitions reduce, it will also reduces the dynamic power dissipation in BS-LFSR. Mathematically,

Pdyn = 1/2 x_{dd}V 2 xi a x CL x Fclki ——— (1)

where, Vi 2 = voltage supply

a = average switching factor CL =load capacitance Fclk=clock frequency,

According to the equation above reducing dynamic power dissipation by changing the power supply and clock frequency will also reduce the circuit's efficiency. In contrast, decreasing the switching activity won't make the circuit perform worse.

By adding extra 2x1 multiplexers plus a normal LFSR, it is possible to create a bit-swapping LFSR [6]. The design

of an n-bit bit-swapped LFSR is shown in Fig.3.2. The multiplexers are

added to the traditional LFSR in order to reorder the patterns and lessen switching activity. Up to 25% fewer transitions can be made overall.

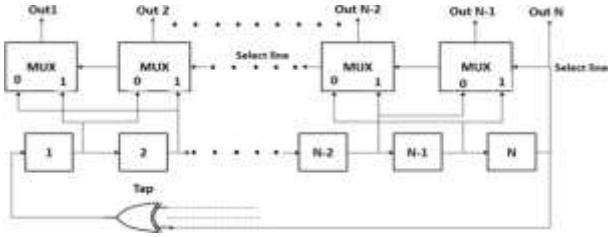

Figure 4: General architecture of BS-LFSR.

3.1.2 OUTPUT RESPONSE ANALYZER

An element of BIST called an Output Response Analyzer examines the outputs obtained from the CUT. The method most frequently used to examine CUT outputs is signature analysis.

(i) Conventional MISR

Signature analysis is carried out using the Multiple Input Signature Register (MISR). Divide the CUT output polynomial by the polynomial of the MISR to perform the MISR's function. The remainder is referred to as the golden signature or reference (manual calculation). The design of a conventional MlSR is shown in Fig. 3.3. Different output polynomials will exist for several output CUTs. Because of this, it will be challenging to analyse the MISR's activity and confirm the golden signature. Additionally, if the number of outputs from the CUT exceeds the number of inputs, this conventional method will not work.

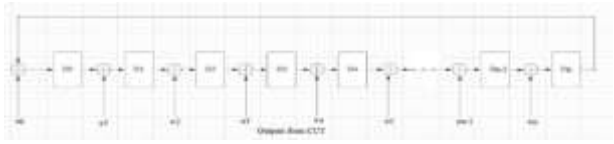

Figure 5: n-bit Conventional MISR.

(ii) Modified MISR

In this MISR, modification is accomplished by aggregating all of CUT's outputs into a single (result) polynomial, which is then fed into a Single Input Signature Register (SISR). All output polynomials are XORed at a point in the modified MISR, as shown in Fig.3.4 (aggregated). Because the resultant is a single polynomial, it is possible to trace the operation of MISR analytically. This MISRi overcomes the disadvantages of conventional MISR, particularly when the number of outputs of CUTs exceeds the number of inputs of MISR.

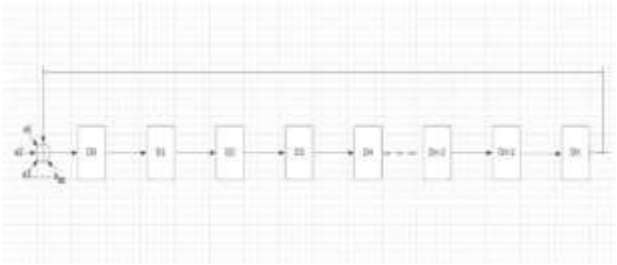

Figure 6: n-bit Modified MISR

3.2 DETERMINING THE POWEREFFICIENCY OF BS-LFSR

Here, we choose 4 bit conventional LFSR and BS-LFSR for determining the power reduction.

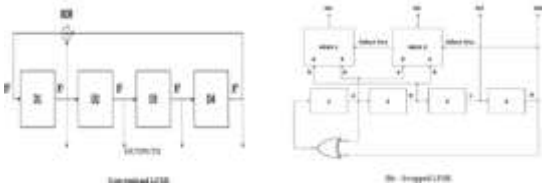

Figure 7: 4 bit conventional LFSR and BS-LFSR

3.2.1 Comparison of LFSR and BS-LFSR Sequence

The conventional LFSR can produce a random sequence by choosing a proper feedback function.The period of sequence is 2n -1 for an n- bit LFSRi and the sequence is continuous and once the 2n -1 different values have occurred, it will repeat for the next sequence.

Similarly, In BS-LFSR, we add extra 2 x 1 multiplexers to the conventional LFSR so as reduce the switching activity or number of transitions. The basic idea is to move two neighbouring bits on a selected line value of the multiplexer. For this, We should consider one of its outputs as selected line(bit n) .If bit n = 1, there should not be any swapping. If bit n = 0,it should swap. Then when n is odd and bit n = 0, bit 1 will be swapped with bit 2, bit 3 with bit 4, and bit n-2 with bit n-1. If n is even and bit n = 0, bit 1 will be swapped with bit 2, bit 3 with bit 4, and bit n-3 with bit n-2.In all cases of the selection line bit n is excluded from the swapping operation. Below shown is the comparison table for initial seed 1001.

Conventional LFSR	BS-LFSR
1 0 0 1	1 0 1 0
0 0 1 0	0 0 1 0
0 1 0 0	0 1 0 0
1 0 0 0	1 0 0 0
0 0 0 1	0 0 0 1
0 0 1 1	0 0 1 1
0 1 1 1	0 1 1 1
1 1 1 1	1 1 1 1
1 1 1 0	1 1 0 1
1 1 0 1	1 1 1 0
1 0 1 0	1 0 0 1
0 1 0 1	0 1 0 1
1 0 1 1	1 0 1 1
0 1 1 0	0 1 1 0
1 1 0 0	1 1 0 0
1 0 0 1	1 0 1 0
Number of transitions	
8 8 8 8	8 8 8 4
Total number of transitions	
32	28

Table 1: Comparison of LFSR and BS-LFSRi Sequence

The number of transitions in table 4.1 is reduced by four because of the switching activity.

As a result, based on equation(1), it will reduce the dynamic power dissipation in the BS- LFSR .

IV. PROPOSED SYSTEM

4.1 Introduction

This paper proposes the design of a power efficient BIST for a combinational circuit and an 8x8 BCD multiplier. The proposed BIST's basic architecture is depicted in Fig.4.1. The TPG in this BIST is BS-LFSR, and the ORA is Modified MISR.

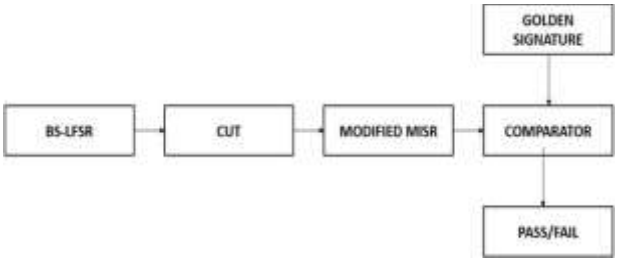

Figure 8: Architecture of proposed BIST

4.2 COMBINATIONAL CIRCUIT AS CUT

4.2.1 BS-LFSR as TPG

If an n-bit maximal length LFSR starts with a non-zero seed and runs for 2n clock cycles to generate all possible test vectors, it will produce a number of transitions equal to 2n−1 transitions at the output of each LFSRi cell. We modify the LFSR by considering one of its outputs (say bit n) to be a selection line that will swap two neighbouring bits elsewhere in the LFSR when the selection line has a specific value (say 0). So if n is odd and bit n = 0, then bit 1 will be swapped with

bit 2, bit 3 with bit 4, ..., bit n − 2 with bit n − 1. If n is even and bit n = 0, then bit 1 will be swapped with bit 2, bit 3 with bit 4, ... , bit n − 3 with bit n − 2. In all cases the selection line, bit n in this case, is excluded from the swapping operation. If bit n = 1, then no swapping is performed.

16 bit BS-LFSR shown in fig 4.2 is achieved by using a conventional LFSR and extra 8x1 multiplexer.

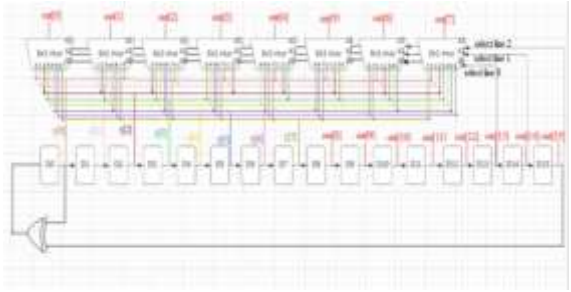

Figure 9: 16-Bit swapped LFSR

4.2.2. Circuit Under Test (CUT)

Fig. 4.3 is the CUT used for the BIST. This combinational circuit has eight outputs O[7:0].The patterns generated by the bit-swapped LFSR (initial seed= "1001010101010110") are input to the CUT.

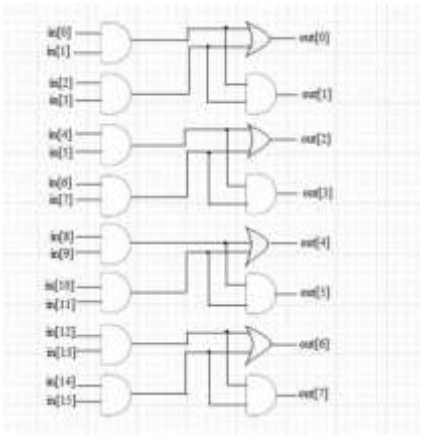

Figure 10: Circuit Under Test (CUT)

4.2.3. Modified MISR as ORA

Fig. 4.4 shows the modified MISRi used for this BIST. Here, the outputs of CUT, i.e., O[7:0] are aggregated (XORed) at a point and the resultant is fed to a SISR.The golden signature for this Modified MISR can be manually calculated by dividing the output polynomial of the CUT by

the MISR polynomial. The remainder obtained gives the golden signature. For the above CUT, the corresponding remainder obtained is x15 + x14 + x13 + x9 + x8 + x6 + x5 + x3 + x + 1 i.e. when written in 16 bits ,the golden signature is 1110001101101011. Similarly, golden signature can be obtained by finding the value of ORA in the 216th clock cycle after the first pattern is produced, for a fault free CUT[17].

Figure 11: 16-Bit Modified MISR.

The proposed BIST is capable of detecting single stuck-at faults in a circuit. Because

this proposed method employs the stuck-at fault model, the circuit contains a single stuck-at fault. In this model, an input or output signal is set to ’0’ or ’1’.

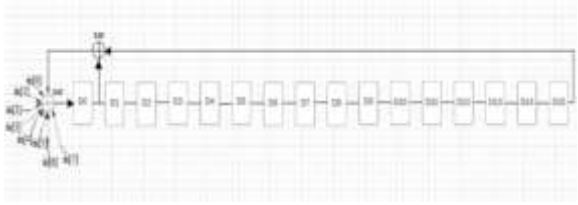

Figure 12: 16- bit Modified MISR

4.2.4 BS-LFSR as TPG

8- bit BS-LFSR shown in fig 4.6 is achieved by using a conventional LFSR and extra 4x1 multiplexers.

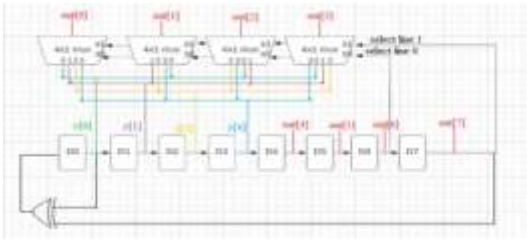

Figure 13: 8-Bit swapped LFSR

4.2.5 Modified MISR as ORA

Fig. 4 . 7 shows the modified MISR used for this BIST. Here, the outputs of 8x8 BCD multiplier (CUT), are aggregated (XORed) at a point and the esultant is fed to a SISR.The golden signature for this Modified MISR can be manually calculated by dividing the output polynomial of the CUT by the MISR polynomial. The remainder obtained gives the golden signature. For the above CUT, the corresponding remainder obtained is x7 + x6 + 1

i.e. when written in 8 bits ,the golden signature is 11000001. Similarly, golden signature can be obtained by finding the value of ORA in the 28th clock cycle after the first pattern is produced, for a fault free CUT[17].

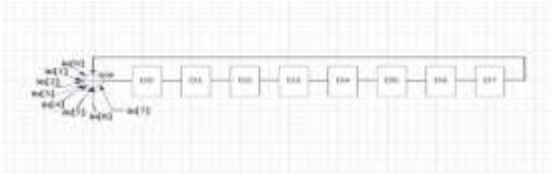

Figure 14 : 8-Bit Modified MISR

V. RESULTS

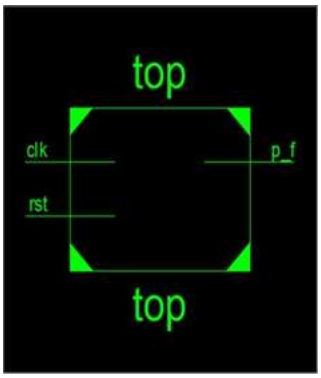

Figure 15. Top View

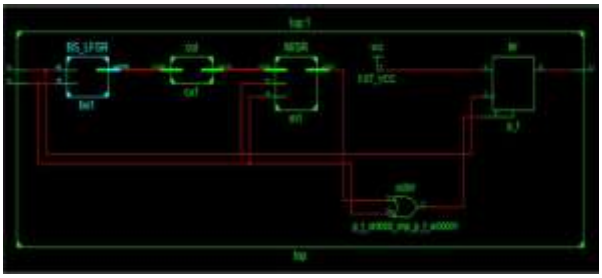

Figure 16. RTL Schematic

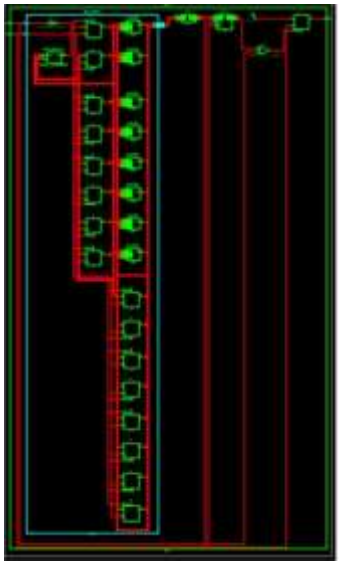

Figure 17. BS_LFSR Top View

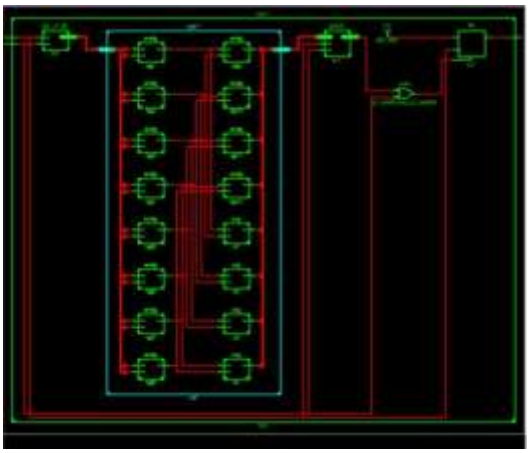

Figure 18. Top View of CUT

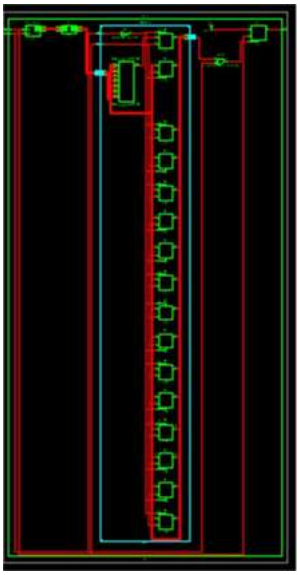

Figure 19. Top View of MISR

Figure 20. BS_LFSR when Reset=0

Figure 21. BS_LFSR when Reset=1

Device Utilization Summary (estimated values)			
Logic Utilization	Used	Available	Utilization
Number of Slices	40	4656	0%
Number of Slice Flip Flops	34	9312	0%
Number of 4 input LUTs	48	9312	0%
Number of bonded IOBs	3	66	4%
Number of GCLKs	1	24	4%

Table 2. Design summary

```
Device utilization summary:
---------------------------

Selected Device : 3s500evq100-5

 Number of Slices:                       40  out of   4656     0%
 Number of Slice Flip Flops:             34  out of   9312     0%
 Number of 4 input LUTs:                 48  out of   9312     0%
 Number of IOs:                           3
 Number of bonded IOBs:                   3  out of     66     4%
 Number of GCLKs:                         1  out of     24     4%


Timing Summary:
---------------
Speed Grade: -5

   Minimum period: 6.380ns (Maximum Frequency: 156.744MHz)
   Minimum input arrival time before clock: 3.046ns
   Maximum output required time after clock: 4.040ns
   Maximum combinational path delay: No path found

Timing Detail:
--------------
All values displayed in nanoseconds (ns)

=========================================================================
Timing constraint: Default period analysis for Clock 'clk'
  Clock period: 6.380ns (frequency: 156.744MHz)
  Total number of paths / destination ports: 202 / 34
-------------------------------------------------------------------------
Delay:               6.380ns (Levels of Logic = 6)
  Source:            bsl/y_15_1 (FF)
  Destination:       ml/y_0 (FF)
  Source Clock:      clk rising
  Destination Clock: clk rising
```

Figure 22. Time summary

Figure shows the time summary of proposed method. Here, the proposed method consumed total 6.380ns of time delay, which is entirely route delay.

VI. CONCLUSION AND FUTURE ENHANCEMENT

This chapter summarizes the major important facets of the present research work.

CONCLUSION

BIST is one of the most popular methods for evaluating circuits since it reduces testing and maintenance costs. BIST does not require additional hardware because it is preprogrammed onto a chip or FPGA. This work uses a bit-swapped LFSR as TPG and a modified MISR as ORA to develop a power-efficient BIST. The BS-LFSR architecture, which augments conventional LFSRs with extra 8x1 and 4x1 multiplexers in accordance with each CUT, improves power efficiency.

The shortcomings of the conventional MISRi were likewise overcome by the modified MISR. The modified MISR can be used on circuits with a larger output to input ratio and helps with the analytical tracing of this MISR's activities. Verilog was used to simulate the results of the Combinational Circuit with and without

halted at faults using Xilinx ISE Design Suite 14.7.This BIST can identify any single stuck-at faults in the circuit because the suggested work is based on the stuck-at fault model; however, the drawback of not being able to identify multiple stuck-at faults in the circuit can be addressed as an additional effort in the future.

Suggestions for Future Work

Even though low power testing methods and various LFSR aspects have been investigated, there are still a lot of uncharted territory to be explored in order to develop new methods that surpass existing ones. In this part, a few possible directions for further testing-related research will be briefly described.

Analyzing the LFSR's Properties

Exploring more features and insights into the behavior of LFSRs could help develop novel techniques that improve test measures like power consumption, fault coverage, and others, as the methodologies in this paper are based on these newfound qualities and insights. Since LFSRs are not just used for testing digital VLSI circuits, many of its characteristics may also be useful in other applications, like encryption.

Check for Low Power Delays

The approach described in the article is based on the most widely used fault model, the stuck-at-fault model. However, delay testing—which is based on a delay fault model—becomes increasingly important to the testing procedure. Delay testing is done to make sure a circuit meets its timing requirements. Compared to the many low power methods that have been proposed for stuck-at-fault model tests, less low power delay testing strategies have been offered, despite the relevance of low power delay in today's systems. Future research should therefore consider different strategies and methodologies to address this problem.

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